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Serial No. 10/708,340
Hiroyuki Akatsu et al.

REMARKS

Claims 8, 10 and 21-23 remain pending in the application. In the Office Action, all claims were rejected under 35 U.S.C. 103(a) as being obvious over U.S. Patent No. 5,481,120 to Mochizuki et al. ("*Mochizuki*") in view of U.S. Patent No. 5,101,256 to Haramé et al ("*Haramé*"). For the reasons set forth below, applicants respectfully submit that the presently pending claims are fully distinguished from the references cited in the final Office Action to reject the claims.

The bipolar transistor as presently recited in claim 8 has a unique feature which does not appear in any prior art of record in the application. The unique feature of the bipolar transistor is that

an opening extends through said first and second dielectric regions, said opening defining edges of said first and second dielectric regions, said edges being aligned in a vertical direction transverse to said lateral directions, said emitter having an edge referenced to said edge of said first dielectric region and said collector pedestal having an edge referenced to said edge of said second dielectric region, such that said emitter is aligned with said collector pedestal.

As argued in response to the preceding Office Action, this unique feature of the transistor recited in claim 8 is only possible because of the way the bipolar transistor is fabricated. Namely, as described illustratively in Paragraph [0055] of the specification, an opening 250 is formed by photolithographic patterning and etching, e.g., RIE, in a layered stack 222 (FIG. 11) (including an oxide layer 236 (first dielectric region), layers 281, 219 and 220) and an underlying silicon nitride layer 270 (second dielectric region). The opening 250 extends through the first and second dielectric regions 236, 270 to the active

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area 202, and as shown in FIG. 12, the opening defines edges of the dielectric regions which are aligned in a vertical direction. The aligned edges of the first and second dielectric regions 236, 270 form a surface on which a vertically extending spacer 272 (FIG. 12) is formed.

The examiner agrees that *Mochizuki* does not teach this feature of the invention, in that "Mochizuki does not expressly teach a (first) dielectric region. . . wherein an opening extends through said (first) dielectric region and defines an edge of said (first) dielectric region to be aligned with the edge of said (second) dielectric region in a vertical direction. . ." (Office Action, p. 3). The examiner apparently also agrees that the secondary reference, *Harame*, does not teach an opening extending through the first and second dielectric regions having vertically aligned edges. In the Office Action (p. 4), *Harame* is cited only as teaching an "opening extends through said (first) dielectric region 28/34/36, said emitter 40 having an edge referenced to said edge of said (first) dielectric region 34/36." Thus, it is clear that neither reference teaches an opening extending through the first and second dielectric regions which has edges aligned in a vertical direction, such as would align the emitter with the collector pedestal.

However, the teachings of *Mochizuki* and *Harame* are then allegedly combined by the examiner to reject the transistor of claim 8 as being obvious. Applicants respectfully traverse this rejection. Applicants respectfully submit that the alleged combination of references does not result in the invention because, in *Harame*, an opening which defines an edge of the first dielectric region is formed by a different lithographic

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processing step than the opening which defines an edge of the second dielectric region. *Mochizuki*, at best, can be said to teach similar processing which does not result in one opening through first and second dielectric regions having edges aligned in a vertical direction. In the combination of references, absent some teaching in the references of simultaneously forming one opening going through both the first and second dielectric regions, there is no reason why an edge of a first opening through a first dielectric region would be aligned in a vertical direction with an edge of a separately formed second opening through a second dielectric region. Thus, the processing steps described in *Mochizuki* and *Haramé*, i.e., considered as a whole, do not result in one opening which extends through both the first and second dielectric regions to define edges of the first and second dielectric regions aligned in the vertical direction.

In the bipolar transistor recited in claim 21, a shallow trench isolation region extends to a depth below the lower surface of the collector pedestal. Applicants traverse the rejection of claim 21 over the combination of *Mochizuki* and *Haramé*. *Haramé* does not teach a structure in which the isolation region 18B/18C (FIG. 1A) extends below the lower surface of the collector pedestal 14. As seen in FIG. 1A, the lower surface of the collector pedestal 14 (where it meets layer 12) and the bottom of the isolation region 18B/18C are at the same depth.

Applicants also traverse the rejection of Claim 22. The vertical edge of the raised extrinsic base 32B clearly is not aligned in a vertical direction with the edge of the opening in a first dielectric region 26/28 (or alternatively an edge of dielectric region 34,

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36A, 36B). Moreover, such edge of the raised extrinsic base 32B is not aligned in the vertical direction with edges of the first and second dielectric regions.

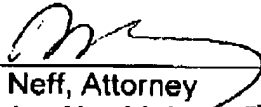
Applicants respectfully submit that claims 10 and 23 are allowable at least based on their dependency from one or more of the above-discussed claims.

For the foregoing reasons, applicants respectfully submit that the present remarks place the application in condition for allowance. If, for any reason, the examiner believes that such action cannot be taken at this time, it is respectfully requested that he telephone the undersigned to discuss any concerns or issues that may remain.

This amendment is filed together with a Request for Continued Examination. It is believed that no other fee is due in connection with the filing of the present response. However, if any fee is due, please debit the Deposit Account No. 09-0458 of the Assignee International Business Machines Corporation.

Respectfully submitted,
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